ST.ANNE'S
COLLEGE OF ENGINEERING AND TECHNOLOGY

(Approved by AICTE, New Delhi. Affiliated to Anna University, Chennai)
(An ISO 9001: 2015 Certified Institution)
ANGUCHETTYPALAYAM, PANRUTI – 607106.

QUESTION BANK

DECEMBER 2018 - MAY 2019 / EVEN SEMESTER

BRANCH: CSE **YR/SEM:** II/IV **BATCH**: 2018 - 2022

SUB CODE/NAME: CS8491-COMPUTER ARCHITECTURE

UNIT 1
PART A

1. List the eight great ideas invented by computer architects ?(Apr/May-2015)
2. What is Multiprogramming or multi tasking?
3. What is meant by clock cycle?
4. Distinguish pipelining from parallelism. ?(Apr/May-2015)
5. Define little Endian arrangement
6. Write down the basic performance equation?(Apr/May-2014)
7. What is relative addressing mode? When is it used?(May/June-12)(Nov/Dec-14)
8. What is indirect addressing mode? Or State the need for indirect addressing mode. Give an example(AM17)
9. Name five parts of the computer components. Or List the major Components of a computer System Apr/May-2017)
9. Distinguish between auto increment and auto decrement addressing mode. (April/May 2010)(M/J-16)
10. State Amdahl's Law.(**Nov/Dec-2014)/AM19**
11. What is Instruction set Architecture? (Nov/Dec-2015)
12. How CPU execution time is calculated? ?(Nov/Dec-2015) (Or) Give the formula for CPU execution time for a program.? (Nov/Dec-2016)
13. How to represent instructions in a computer system?(May/June-2016)
14. List the major components of a computer system.?(April-May17)
15. State the need for indirect addressing mode.give an examples(April-May17)
16. What is instruction set architecture?(Nov-Dec2015).
17. How CPU execution time for a program is calculated?(13)(Nov-Dec15)
18. Define pipelining?
19. What is application and system software?
20. Suppose that we are considering an enhancement to the processor of a server system used for Web Serving. The new CPU is 10 times faster on computation in the Web serving application than the original processor. Assuming that the original CPU is busy with computation 40% of the time and is waiting for I/0 60% of the time, what is the overall speedup gained by incorporating the enhancement?

PART B

Functional Units

1.Give detail description about Components of a computer system with neat diagram. (13)(**ND15)AM19**

2. i.Explain the eight ideas of the Computer architecture which empowered the computer design over the past decades. (7**)AM19**

ii. Tabulate the difference between the RISC and CISC processor.(8)**AM19**

Basic Operational Concepts

1.Explain the basic operational concepts with example**?(april/may17)**

Performance

1. State the CPU performance equation and discuss the factors that affect performance (13)

2.Explain the important measure of the performance of a computer and derive the basic performance equation?(13) (April-May17).

Instructions: Language of the Computer
1..Explain the various techniques to represent instructions in a computer system?(13)(April-May15).

Operations, Operands
1.Explain the types of operations and operands with example?

Instruction representation
1.How will you represent a instructions in computer architecture with example?

Logical operations
1.Explain the logical operation with example?(april/may16)

Decision making
1.Explain the types of decision making with suitable example?

MIPS Addressing.
1.Explain the types of MIPS addressing modes with example?**AM19**

PARTC

1.Explain the types od addressing modes with examples**?(APRIL/MAY15)AM19**

2.Explain the basic components of computer system with block diagram?

UNIT II

PART A

1. What is ALU? What is its use?
2. Which are the two basic data types implemented in the computer system?
3. What is fixed point number system?
4. What is floating point number system?
5. What is signed magnitude representation?
6. Define little Endian arrangements?(nov/dec14)
7. How do you relate addition and subtraction?
8. What is half adder? (apr/may09)
9. Draw the full adder circuits using two half adders?(nov/dec7)
10. Draw a full adder circuits and gives the truth table? (apr/may7)
11. What is ripple carry adder? (apr/may15)
12. Discuss the principle behind the booth algorithm?(apr/may17)
13. Define overflow rule in addition ? (nov/dec09)
14. Discuss the role of booth algorithm in the design of fast multipliers? (apr/may16)
15. Define IEEE floating point single and double precision standard? (nov/dec6,7)
16. What is the advantage of non restoring over restoring division?
17. State the rule for floating point division?
18. What do you mean by guard bits?
19. State commonly used method of truncations?
20. What is sub word parallelism ?(apr/may15)
21. State the representation of double precision floating point numbers?(nov/dec15)
22. How overflow occur in subtraction?(may15)

23. What is carry lookahead adder? **(dec14)**
24. Comparision between restoring and non restoring division algorithm? (may/12)
25. Define underflow and overflow?
26. Define normalization?
27. write the rules for multiplication**?**
28. Write the rules for division?
29. Find 1's complements of(10101100)?
30. Find 2,s complements of(01011011) **?**

PART B

Addition and Subtraction

1.Design a 4bit binary adder /subtractor and explain its function ?
2.Design a 4 bit adder and explain its functions in detail? (may10)
3.Explain the principles of carrylook ahead adder?(may11)

Multiplication

1.Explain the sequential version of multiplication algorithm and is hardware ?(may15)
2.Explain in detail about the multiplication algorithm with suitable examples and diagram ? (dec15)
3.Explain the booth multiplication algorthim of signed two's complements numbers ? (nov/dec16)
4. Calculate the following problems using BOOTH'S ALGORITHM (13)

(i) (+13) x(–6)
(ii) (+13) x (+6)
(iii) (-13) x (-6)
(iv)(-13) x (+6) **AM19**

5.Calculate 10011 (-13) x 01011 (+11) using Signed-Operand Multiplication. (13) **AM19** (13)

Division

1.Discuss in detail about division algorithm in detail with diagram and examples? (nov/dec15)

Floating Point Representation

1.Explain how floating point addition is carried out in a computer system .Give an example for a binary floating point addition?

Floating Point Operations

1.Explain the types of Floating Point Operations?
2.Explain how floating point addition is carried out in a computer system.give an example for a binary floating point addition?(may2015)

Subword Parallelism

1.Explain In detail about the the Subword Parallelism ?

PARTC

1.Explain the booth multiplication algorithm with example?
2.Explain the restoring division algorthim with example?
3. Explain the non restoring division algorthim with example?
4.Explain the IEEE standard floating point representation ?

UNIT 3

PART- A

1. Define MIPS?
2. Define MIPS rate?
3. Define parallel processing?
4. Define pipelining? (may17)
5.What is instruction pipelining?
6.List the four stages in the instruction pipelining?
7. Define datapath?
8. Define register file?
9. what are hazard?
10.Define structural hazard? (may14)
11.Define instruction hazard?
12.What is control hazard? (may12,13)
13.What are R-type instruction? (may-15)
14.What is branch prediction? (dec-15)
15.What is a hazard? What are its types? (dec-15)
16.What is data hazard? (may13)

17.Why branch prediction algorithm neded? (ma y12)
18.What is meant by speculative execution? (may12)
19. What is branch target/prediction buffer? (may15)
20.Different static and dynamic branch prediction? (may13)
21.What is the role of cache in pipelining? (dec-11)
22.What is branch instruction?
23.What is load and store insruction?
24.Define clock skewing?
25.Define instruction throughput?
26. What is operand forwarding?
27.What is an instruction queue and prefetching?
28. Define exception?
29.What are the types of exception?
30.What are the classification of data hazards?

PART B

1. Explain the basic concepts of pipelining? (dec-09)
2. Explain the basic operations of a four stage pipelining with a neat diagram? (dec-9)
3.Discuss the various hazard that might arise in pipeline? (dec-09)
4.What is instruction hazard? Explain the methods for dealing with instruction hazard?(may10)
5. What are the hazards of conditional branches in pipelines? How it can be resolved?(may-11).
6.Explain the different types of pipeline hazards with example? (may15,dec17)
7.Explain the data hazards with example?
8.Discuss the basic concepts of pipelining? (may12)
9.Explain the basic operation of four stage pipelining with neat diagram? (may-13)
10. Describe the techniques for handling control hazards in pipelining? (may13)
11**.** Describe the dynamic branch prediction techniques? (May-13)
12**.** Explain the basics MIPS implementation with necessary multiplexiers and control lines?**dec-15) AM19**
13.Explain in detail how exception are handled in MIPS architecture? (may-15)
14.Explain how instruction pipeline works? What are the various situation where an instruction pipeline can stall with example? (**may-15)AM19**

PART- C

1.Write a briefly about MIPS implementation with suitable diagram (may-17)
2.Explain the different types of pipeline hazards with example? (May-18)
3.Explain how handling data and control hazard with example? (Dec-17)
4.Describe the dynamic branch prediction.?

UNIT IV

PART- A

1. Describe the main idea of ILP. ?
2.List the three important properties of vector instructions. ?
3. Analyze the main characteristics of SMT processor ?
4. Define VLIW processor.?
5. Express anti-dependence. How is it removed?
6. State the efficiency of superscalar processor?
7. Differentiate between strong scaling and weak scaling ?
8. Show the performance of cluster organization ?
9. Compare SMT and hardware multithreading.?
10. Define the Flynn classification?
11. Integrate the ideas of in-order execution and out-of-order execution. ?
12. Discriminate UMA and NUMA?
13. Express the need for instruction level parallelism?
14. Formulate the various approaches to hardware multithreading?
15. Categorize the various multithreading options?
16. Differentiatefine grained multithreading and coarse grained multithreading?
17. Classify shared memory multiprocessor based on the memory access latency ?
18. Define parallel processing?

19. Define multiprocessor system?
20. Define parallel processing program?
21. What is cluster?
22. What Is Multicore?
23. What is CMP and SMP?
24. State Amdahl's law?
25. What is the use of Amdahl's law?
26. What is strong scaling?
27. What is weak scaling?
28. What is SISD?
29. What is SIMD?
30. What is MISD?

PART- B

Instruction-level-parallelism

i)Define parallelism and its types? (4)

ii)List the main characteristic of instruction level parallelism (9)

Parallel processing challenges

1.Give the concept of parallel processing? (4)

2.summarize the challenges faced b parallel processing? (9)

Flynn's classification

1.Explain flyn's classification in detail? **AM19**

SISD, MIMD, SIMD, SPMD

1. Elaboratein detail about the following

i).SISD.

ii).MIMD

iii) **SIMD**

iv) SPMD

Vector Architectures

1.Explain the vector architecture in details?

2.Discuss the following in detail (7)

i). Vector processor. (6)

ii).Superscalar processor.

Hardware multithreading

1.Express in detail about hardware multithreading.

2.Discuss the principle of hardware multithreading and elaborate its types **AM19**

Multicore processors Shared Memory

1. What are multicore processors and explain it

2.i) Evaluate the features of Multicore processors. (6)

ii) How message passing is implemented in Multiprocessors (7)

MultiprocessorsIntroduction to Graphics Processing UnitsClusters,

i)Describe about Graphics Processing unit (5)

ii) Discuss about cluster and warehouse architecture (8)

Warehouse Scale Computers

1.Explain the warehouse scale computers?

Other Message-Passing Multiprocessors ?

1.Explain the message passing multiprocessor?

PART C

1. Explain flyn's classification in detail?**AM19**
2. Explain in detail about hardware multithreading? **AM19**
3. Explain instruction level parallel processing ? state the challenges of parallel processing?

UNIT 5

PART A

1. What is principle of locality?
2. Define spatial locality?
3. Define Memory Hierarchy?
4. Define hit ratio. (A.U.APR/MAY 2013,NOV/DEC 2015)
5. What is TLB? What is its significance?
6. Define temporal locality.
7. How cache memory is used to reduce the execution time. (APR/MAY'10)
8. Define memory interleaving. (A.U.MAY/JUNE '11) (apr/may2017)
9. Define Hit and Miss? (DEC 2013)
10. What is cache memory?NOV/DEC 2016
11. What is memory system? [MAY/JUNE '11] [APR/MAY 2012]
12. What is Read Access Time? [APR/MAY 2012]
13. What is the necessary of virtual memory? State the advantages of virtual memory? MAY/JUNE 2016.
14. What are the units of an interface? (Dec 2012)
15. Distinguish between isolated and memory mapped I/O? (May 2013)
16. Distinguish between memory mapped I/O and I/O mapped I/O.
17. Define virtual memory.(nov/dec 2017)
18. What is Semi Random Access?
19. What is the use of DMA? (Dec 2012)(Dec 2013,APR/MAY2018)
20. Mention the advantages of USB. (May 2013)
21. What is meant by vectored interrupt?(Dec 2013)
22. Compare Static RAM and Dynamic RAM.(Dec 2013,APR/MAY2018)
23. what is DMA ?(NOV/DEC 2014)
24. Differentiate programmed I/O and interrupt i/O..(NOV/DEC2014)
25. what is the purpose of dirty /modified bit in cache memory.(NOV/DEC2014)
26. Define miss rate
27. Define miss penalty
28. Define tag in TLB
29. What is write back cache
30. What are the techniques to improve cache performance?

PART B

Memory Hierarchy

1.Expain in detail about memory Hierarchy with neat diagram

Memory technologies

1.Expain in detail about memory technologies **?**

Cache memory

1. Discuss the various mapping schemes used in cache memory
2. Explain mapping functions in cache memory in cache memory to determine how memory blocks are placed in cache **AM19**
3. Explain the various mapping techniques associated with cache memories

Measuring and improving cache performance

1. Discuss the methods used to measure and improve the performance of the cache

Virtual memory, TLB's

1. Explain the virtual memory address translation and TLB with necessary diagram.

Accessing I/O Devices

1. Describe in detail about programmed Input/Output with neat diagram

2. Describe in detail about programmed Input/Output with neat diagram

3. Explain about input-output processor (IOP) (**5)AM19**

Interrupts

1. Explain sequence of operations carried on by a processor when interrupted by a peripheral device connected to it(MAY/JUN 2018).

2. Explain the interrupt priority scheme with diagram?

3. Explain in detail about interrupts with diagram

Direct Memory Access

1. Draw the typical block diagram of a DMA controller and explain how it is used for direct data transfer between memory and peripherals.

2. With a neat sketch explain the working principle of DMA. (8)**AM19**

Bus structure

1. Explain the bus structure with block diagram?

Bus operation

1.Explain the asynchronous and synchronous bus in bus operation?

Arbitration

1. Explain the types of bus arbitration?
2. Explain the centralized bus arbitration?
3. Explain the distributed bus arbitration?

Interface circuits

1.Explain the serial and parallel port?

USB.

1.Explain the USB in detail in diagram?

PART C

PART C — (1 x 15 = 15 marks)

(a) In a small town, there are three temples in a row and a well in front of each temple. A pilgrim came to the town with certain number of flowers.

Before entering the first temple, he washed all the flowers he had with the water of well. To his surprise, flowers doubled. He offered few flowers to the God in the first temple and moved to the second temple. Here also, before entering the temple he washed the remaining flowers with the water of well. And again his flowers doubled. He offered few flowers to the God in second temple and moved to the third temple. Here also, his flowers doubled after washing them with water. He offered few flowers to the God in third temple.

There were no flowers left when pilgrim came out of third temple and he offered same number of flowers to the God in all three temples. What is the minimum number of flowers the pilgrim had initially (X)? And find the value of (X/3) using Restoring Division method? How many flower did he offer to each God (Y)? And find the value of (Y/3) using Non-Restoring Division method?

Or

(b) (i) You have been asked to design a cache with the following properties : (8)

(1) Data words are 32 bits each
(2) A cache block will contain 2048 bits of data
(3) The cache is direct mapped
(4) The address supplied from the CPU is 32 bits long
(5) There are 2048 blocks in the cache
(6) Addresses are to the word.

(ii) In the below picture, there are 8 fields (labeled a, b, c, d, e, f, g, and h), you will need to indicate the proper name or number of bits for a particular portion of this cache configuration. Explain the process of accessing data using this design. (7)